IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating ~~each~~ at least one of the ~~plurality of~~ binary outputs ~~as a~~ as an elementary EXOR symmetric function of the binary inputs;

wherein the elementary EXOR symmetric function comprises the result of EXOR logic combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of inputs is an odd number or AND logic combining sets of one or more binary inputs and EXOR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, ~~wherein~~ said logic circuit is divided into a plurality of EXOR logic units, each EXOR logic unit is arranged to generate logic unit binary outputs ~~as a~~ as an elementary EXOR symmetric function of the binary inputs to the EXOR logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said EXOR logic units, ~~and the~~ and at least one binary ~~outputs~~ output of said plurality of outputs ~~are~~ is generated using said logic unit binary outputs of a plurality of said EXOR logic units.

2. (Currently Amended) A parallel counter according to claim 1, wherein said logic circuit is arranged to generate at least one of the binary outputs as an elementary OR symmetric function of the binary inputs, and is divided into a plurality of OR logic units, the binary inputs of said plurality of inputs are divided according to a binary tree into inputs into a plurality of said OR logic ~~units.~~ units, each OR logic unit is arranged to generate at least one logic unit binary output as an elementary OR symmetric function of the binary inputs to the OR logic unit, the

binary inputs of said plurality of inputs are divided into inputs into a plurality of said OR logic units, at least one binary output of said plurality of outputs is generated using said logic unit binary outputs of a plurality of said OR logic units, and the elementary OR symmetric function comprises the result of OR logic combining binary inputs to generate a binary output which is high if and only if m >1 or AND logic combining sets of binary inputs and OR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k,

3. (Currently Amended) A parallel counter according to ~~claim 1~~ claim 2, wherein said OR logic units are arranged to receive 2^n of said binary inputs, where n is an integer indicating the level of the OR logic units in the binary tree, said logic circuit has m OR logic units at each level, where m is a rounded up integer determined from (the number of binary inputs)/ 2^n, OR logic units having a higher level in the binary tree comprise logic of OR logic units at lower levels in the binary tree, and each OR logic unit is arranged to generate logic unit binary outputs ~~as a~~ as an elementary OR symmetric function of the binary inputs to the OR logic unit.

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Currently Amended) A logic circuit for multiplying two binary numbers comprising:

array generation logic for generating an array of binary numbers comprising all possible combinations of each bit of each binary number;

array reduction logic including at least one parallel counter ~~according to any preceding claim~~ for reducing the number of combinations in the array; and

binary addition logic for adding the reduced combinations to generate an ~~output.~~ output;

wherein at least one said parallel counter comprises:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating at least one of the binary outputs as an elementary EXOR symmetric function of the binary inputs;

wherein the elementary EXOR symmetric function comprises the result of EXOR logic combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of inputs is an odd number or AND logic combining sets of one or more binary inputs and EXOR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, said logic circuit is divided into a plurality of EXOR logic units, each EXOR logic unit is arranged to

generate logic unit binary outputs as an elementary EXOR symmetric function of the binary inputs to the EXOR logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said EXOR logic units, and at least one binary output of said plurality of outputs is generated using said logic unit binary outputs of a plurality of said EXOR logic units.

17. (Original) A method of designing a logic circuit comprising:

providing a library of logic module designs each for performing a small symmetric function;

designing a logic circuit to perform a large symmetric function;

identifying small symmetric functions which can perform said symmetric function;

selecting logic modules from said library to perform said small symmetric functions;

identifying a logic circuit in the selected logic circuit which performs a symmetric function and which can be used to perform another symmetric function;

selecting the logic circuit corresponding to the identified symmetric function and using the selected logic circuit with inverters to perform said other symmetric function using the relationship between the symmetric functions:

$$OR\_n\_k(X_1...X_n) = \neg OR\_n\_(n+1-k)(\neg X_1...\neg X_n)$$

where $\neg$ denotes an inversion, n is the number of inputs, and k is the number of sets of inputs AND combined together.

18. (Currently Amended) A conditional parallel counter having m possible high inputs out of n inputs, where m<n, and n and m are integers, the counter ~~comprising the~~ comprising a parallel counter ~~according to claim 1~~ for counting inputs to generate p outputs for m inputs, wherein the number n of inputs to the counter is greater ~~than 2^p.~~ than 2^p, and said parallel counter comprises:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating at least one of the binary outputs as an elementary EXOR symmetric function of the binary inputs;

wherein the elementary EXOR symmetric function comprises the result of EXOR logic combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of inputs is an odd number or AND logic combining sets of one or more binary inputs and EXOR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, said logic circuit is divided into a plurality of EXOR logic units, each EXOR logic unit is arranged to generate logic unit binary outputs as an elementary EXOR symmetric function of the binary inputs to the EXOR logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said EXOR logic units, and at least one binary output of said plurality of outputs is generated using said logic unit binary outputs of a plurality of said EXOR logic units.

19. (Currently Amended) A constant multiplier comprising a conditional parallel counter having m possible high inputs out of n inputs, where m<n, and n and m are integers, the counter ~~comprising the~~ comprising a parallel counter ~~according to claim 1~~ for counting inputs to generate p outputs for m inputs, wherein the number n of inputs to the counter is greater ~~than 2^p.~~ than 2^p, and said parallel counter comprises:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating at least one of the binary outputs as an elementary EXOR symmetric function of the binary inputs;

wherein the elementary EXOR symmetric function comprises the result of EXOR logic combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of inputs is an odd number or AND logic combining sets of one or more binary inputs and EXOR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, said logic circuit is divided into a plurality of EXOR logic units, each EXOR logic unit is arranged to

generate logic unit binary outputs as an elementary EXOR symmetric function of the binary inputs to the EXOR logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said EXOR logic units, and at least one binary output of said plurality of outputs is generated using said logic unit binary outputs of a plurality of said EXOR logic units.

20. (Currently Amended) A digital filter comprising a conditional parallel counter having m possible high inputs out of n inputs, where m<n, and n and m are integers, the counter ~~comprising the~~ comprising a parallel counter ~~according to claim 1~~ for counting inputs to generate p outputs for m inputs, wherein the number n of inputs to the counter is greater ~~than 2^p.~~ than 2^p, and said parallel counter comprises:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating at least one of the binary outputs as an elementary EXOR symmetric function of the binary inputs;

wherein the elementary EXOR symmetric function comprises the result of EXOR logic combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of inputs is an odd number or AND logic combining sets of one or more binary inputs and EXOR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, said logic circuit is divided into a plurality of EXOR logic units, each EXOR logic unit is arranged to generate logic unit binary outputs as an elementary EXOR symmetric function of the binary inputs to the EXOR logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said EXOR logic units, and at least one binary output of said plurality of outputs is generated using said logic unit binary outputs of a plurality of said EXOR logic units.

21. (Currently Amended) A parallel counter comprising:

~~a plurality of~~ at least five inputs for receiving a binary number as a plurality of binary inputs;

~~a plurality of~~ at least three outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for ~~generating each~~ generating at least two of the plurality of binary outputs ~~as a~~ as elementary EXOR symmetric ~~function~~ functions of the binary ~~inputs.~~ inputs, wherein the elementary EXOR symmetric function comprises the result of EXOR logic combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of inputs is an odd number or AND logic combining sets of one or more binary inputs and EXOR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs.

22. (Currently Amended) A parallel counter according to claim 21 wherein said logic circuit is arranged to generate ~~at least one of the~~ first and second binary outputs ~~as a~~ as elementary EXOR symmetric functions of the binary inputs ~~using exclusive OR logic for combining a plurality of sets of one or more binary inputs~~.

23. (Currently Amended) A parallel counter according to claim 22 wherein said logic circuit is arranged to generate the first binary output as the elementary EXOR symmetric function comprising the result of EXOR logic combining the binary inputs, and to generate the second binary output as the elementary EXOR symmetric function comprising the result of ~~logically~~ AND logic combining members of each set of binary inputs and ~~to logically~~ exclusively OR logic combining the result of the AND operations.

24. (Currently Amended) A parallel counter according to ~~claim 23~~ claim 21 wherein said logic circuit is arranged to generate the first binary output by EXOR logic combining the binary inputs to and generate at least one $(i+1)^{th}$ binary output by ~~logically~~ AND logic combining 2^i of the binary inputs in each set and EXOR logic combining the result of the AND logic

combinations ~~for the generation of the ith binary output~~, where i is an integer from 1 to N-1, N is the number of binary outputs and i represents the significance ~~of each~~ of a binary output, each set being unique and the sets covering all possible combinations of binary inputs.

25. (Canceled)

26. (Currently Amended) A parallel counter according to claim 21 wherein said logic circuit is arranged to generate at least one of the binary outputs ~~as a~~ as an elementary OR symmetric function of the binary inputs ~~using OR logic for combining a plurality of sets of one or more binary inputs.~~ wherein the elementary OR symmetric function comprises the result of OR logic combining binary inputs to generate a binary output which is high if and only if m >1 or AND logic combining sets of binary inputs and OR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k,

27. (Canceled)

28. (Currently Amended) A parallel counter according to ~~claim 27~~ claim 26 wherein said logic circuit is arranged to generate the Nth binary output as an elementary OR symmetric function comprising the result of ~~logically~~ AND logic combining 2^{N-1} of the binary inputs in each set ~~for the generation of the Nth binary output~~ and OR logic combining the AND logic combined sets of binary inputs, where N is the number of binary outputs and the Nth binary output is the most significant, each set being unique and the sets covering all possible combinations of binary inputs.

29. (Canceled)

30. (Currently Amended) A parallel counter according to claim 21 wherein said logic circuit is arranged to generate a first binary output ~~as a~~ as an elementary EXOR symmetric function of the binary inputs ~~using exclusive OR logic for combining a plurality of sets of one or more binary inputs~~, and to generate an Nth binary output ~~as a~~ as an elementary OR symmetric function

of the binary inputs ~~using OR logic for combining a plurality of sets of one or more binary inputs.~~, wherein the elementary OR symmetric function comprises the result of OR logic combining binary inputs to generate a binary output which is high if and only if m >1 or AND logic combining sets of binary inputs and OR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k,

31. (Currently Amended) A parallel counter according to claim 21 wherein said logic circuit is arranged to generate two possible binary outputs for a binary output less significant than the N^{th} binary output, as elementary OR symmetric functions of the binary inputs ~~using OR logic for combining a plurality of sets of one or more binary inputs~~ where N is the number of binary outputs, the sets used for each possible binary output being of two different sizes which are a function of the binary output being generated; and said logic circuit including selector logic to select one of the possible binary outputs based on a more significant binary output value.

32. (Currently Amended) A parallel counter according to claim 31 wherein said logic circuit is arranged to generate the two possible binary outputs for the $(N-1)^{th}$ binary output less significant than the N^{th} binary output, as elementary OR symmetric functions of the binary inputs ~~using OR logic for combining a plurality of sets of one or more binary inputs~~, the sets used for each possible binary output being of size $2^{N-1} + 2^{N-2}$ and 2^{N-2} respectively and said selector logic being arranged to select one of the possible binary outputs based on the N^{th} binary output value.

33. (Currently Amended) A parallel counter according to claim 21 wherein said logic circuit includes a plurality of subcircuit logic modules each generating intermediate binary outputs ~~as a~~ as an elementary OR or EXOR symmetric function of some of the binary inputs, and logic for logically combining the intermediate binary outputs to generate said binary outputs.

34. (Canceled)

35. (Canceled)

36. (Canceled)

37. (Canceled)

38. (Canceled)

39. (Canceled)

40. (Canceled)

41. A logic circuit ~~according to claim 40~~ for multiplying two N bit binary numbers, the logic circuit comprising:

array generation logic for performing the logical AND operation between each bit in one binary number and each bit in the other binary number to generate an array of logical AND combination comprising an array of binary values, and for further logically combining the generated values to generate an array in which the maximal depth of the array is below N bits;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the two binary numbers;

wherein said array reduction logic includes at least one parallel counter according to claim 1, 2, 3, 21, 22, 23, 24, 26, 28, 30, 31, 32, or 33.